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A Digital Circuit for Jitter Reduction of GPS-disciplined 1-pps Synchronization Signals

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Abstract *– The Global Positioning System (GPS) satellites transfer accurate time from atomic clocks, thus enabling the receivers on Earth to produce high-stability synchronization signals (i.e., trains of low-jitter pulses without drift). The timing accuracy of the generated stream of pulses depends on the features as well as on the cost of the specific GPS receiver employed. This paper describes a fully digital synchronization circuit that is able to reduce the jitter associated to the 1 pulse per second (1-pps) signal generated by a typical low-cost receiver of moderate timing accuracy within a short settling time interval. The proposed circuit has been implemented using an FPGA and the jitter reduction has been estimated experimentally.*

Keywords *– GPS, synchronization, jitter measurements, phase lock loops, 1-pps, signal processing.*

I. INTRODUCTION

Global time synchronization concerns with the distribution of time or frequency values to multiple clocks. Global time synchronization has been playing a central role in computer and digital telecommunication networking for several years [1]–[4]. In fact, circuit-switched data networks require stringent synchronization between nodes in order to avoid slips that may be harmful for some data services [5]. In last years several standards have been released by the International Telecommunication Union - Telecommunication Sector (ITU-T) and by the European Telecommunication Standard Institute (ETSI) to manage the synchronization problem [6]–[8]. More recently, assuring appropriate time synchronization has also become critically important for distributed measurement and automation purposes as well as for some pervasive computing applications based on embedded devices, such as the wireless sensor networks [9]–[10]. Generally, the problem of assuring a suitable synchronization at the network level is addressed by specific time distribution protocols, such as the IEEE 1588 Precision Time Protocol (PTP) or the Network Time Protocol (NTP). An alternative and well-known approach is based on the use of the Global Positioning System (GPS). The GPS consists of a constellation of 24 satellites equipped with atomic clocks whose time values can be used for synchronizing multiple clocks over wide geographical areas [11]–[12]. A typical GPS receiver consists of a radio module, a demodulator and a micro-controller. Once it is turned on, a receiver at first computes its space coordinates (i.e. latitude, longitude, and altitude) using the data collected from different satellites; then it starts generating a low-jitter 1 pulse per second (1-pps) signal, as well as other possible standard frequency output signals (e.g. 1, 5, or 10 MHz), by locking its internal clock with time information received from the satellites. In particular, the simplest GPS receivers have just one channel and establish connections with multiple satellites according to a fast-switching sequential scheme. Conversely, more involved models assign a different channel to each satellite in view (i.e. above the horizon), thus performing simultaneous acquisitions. In most GPS receivers, the worst-case short-term period fluctuations of the 1-pps signal is in the order of some tens of ns, which means relative frequency variations in the order of 10^{-7}. In essence 1-pps constitutes a perfect frequency signal with some residual jitter. The amount of jitter can be reduced by averaging the time values received simultaneously from different satellites over a certain time interval (e.g. 24 hours) [13]. While the latter approach is essential for fundamental metrological purposes [14]–[15], a jitter of about ±100 ns is suitable in most consumer and industrial applications. Nonetheless, if a lower jitter is required (e.g. in mobile or wired long-haul communications networks), special locking circuits exist to reduce the period variations of the native 1-pps stream. Such circuits are conceived to improve the GPS-based synchronization at the physical layer regardless of the specific communication mechanism between systems. In contrast, protocol-based synchronization schemes, such as the IEEE 1588, operate at higher layers, and rely mostly on software signal processing techniques. In this paper a fully digital synchronization circuit to reduce the jitter affecting the 1-pps signal generated by typical low-cost GPS receivers is proposed. In Section II the architecture of the synchronization circuit and its principle of operation as well as its advantages and limitations in comparison with other high-accuracy existing solutions are described. Then, in Section III the main results of the experimental activity are reported. Finally, some conclusions are discussed in Section IV.

II. THE SYNCHRONIZATION CIRCUIT

One of the most effective techniques to synthesize a stable 1-pps synchronization signal from a GPS receiver relies on special Phase Lock Loops (PLLs) including both a Proportional-Integral-Derivative (PID) controller and a high-stability Temperature Compensated Voltage Controlled Crystal Oscillator (TCVCXO), as shown in Fig. 1 [16]-[18]. Such disciplined crystal oscillators are usually characterized by a very high short-term stability and locked to the time of the atomic clocks of the GPS constellation by continuously measuring and compensating the phase shift between the output 1-pps stream and the input 1-pps signal through the PID controller that in turn drives a varactor diode inside the TCVCXO. In such a way, high long-term 1-pps stability can be achieved. The disciplined TCVCXO technology provides very stable signals, i.e. with a jitter in the order of a few ns. Unfortunately, the disciplined TCVCXO systems suffer from three major disadvantages, i.e.:

1. They are based on a mixed analog-digital technology;
2. They require a quite long settling time to lock the signal at best of their accuracy (i.e. in the order of some hours);
3. They are expensive, thus being unsuitable for low-cost pervasive applications.

Such issues can be effectively tackled at the expense of a lower timing accuracy using the proposed synchronization circuit. The block diagram of such a circuit is shown in Fig. 2. The circuit is fully digital and clocked by a plain crystal oscillator (XO). Its architecture is similar to a digital PLL, although it is specifically optimized for locking 1-pps signals through a Proportional and Integral (PI) digital controller. In fact, the coefficients of the PI controller are set to achieve a settling time much shorter than in TCVCXO-based solutions (i.e. in the order of a few tens of seconds). Notice that the input binary 1-pps signal is sampled by the system clock XO through a simple flip-flop (i.e. without any Analog-to-Digital converter).

In brief, the system operation consists of two subsequent stages. In the former phase (*transient phase*), immediately after turning the system on, the PI controller is disabled and the Counter 1 measures the average period of the input 1-pps signal over a user-defined number of periods N, in order to provide an initial estimate of the regenerated output 1-pps signal period, which is stored into the Counter 2. This is beneficial in order to shorten the locking latency of the circuit. Afterwards, in the *locking phase*, the Counter 1 is switched to measure the delay between the output and the input 1-pps signals. Such a delay is sent to the PI controller which in turn adjusts the period of the output 1-pps signal to track possible input period variations.

A. Analysis of the transient phase

Let T_C be the nominal period of the XO. If we refer to:

- T_{ID} as the ideal period of the 1-pps signal;
- Δ_{IN_i} as the period variation of the input signal at the ith second of operation;

the actual input period at time i is $T_{IN_i} = T_{ID} + \Delta_{IN_i}$ and the average period of the input 1-pps signal during the *transient phase* results from:

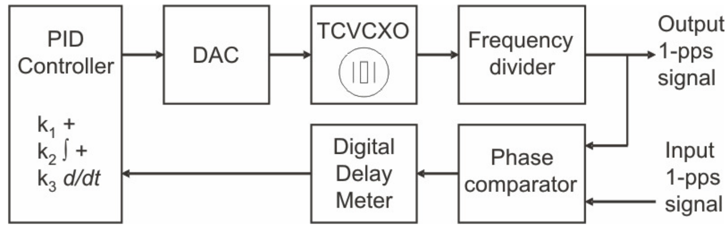

Fig. 1 – A typical high-accuracy GPS synchronization circuit based on disciplined VCXO technology.

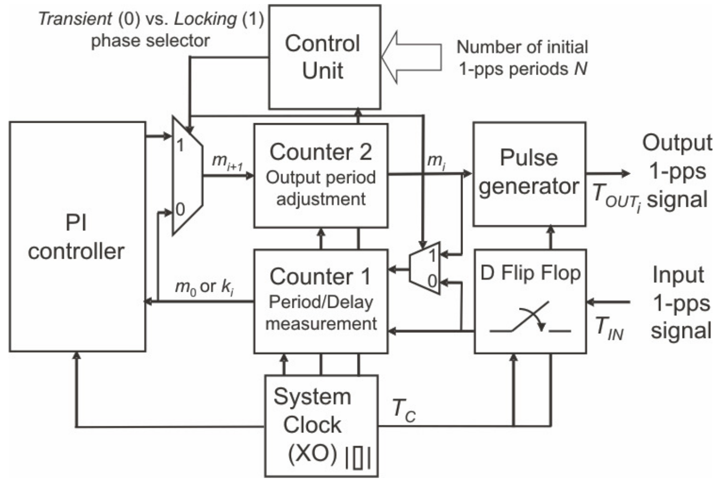

Fig. 2 – Architecture of the proposed synchronization circuit.

$$\overline{T}_{IN} = T_{ID} + \frac{1}{N}\sum_{i=1}^{N} \Delta_{IN_i} \qquad (1)$$

Given that the input period duration is measured in terms of ticks of the Counter 1, (1) can be expressed also as

$$\overline{T}_{IN} = \frac{T_C}{N}\cdot\sum_{i=1}^{N} n_i = \left(m_0 + \frac{1}{N}\cdot\sum_{i=1}^{N}\Delta n_i\right)\cdot T_C \qquad (2)$$

where m_0 is the integer part of the ratio between the total number of counts and the amount of collected periods N, n_i is the number of ticks associated to the ith period and the terms $\Delta n_i T_C$ represent the estimated values of Δ_{IN_i}. If the values of Δ_{IN_i} are assumed to be normally distributed with standard deviation $\sigma_{T_{IN}}$, the period of the output 1-pps signal at the end of the *transient phase* can be set equal to $T_{OUT_0} = m_0 \cdot T_C$ with accuracy smaller than T_C (e.g. εT_C with $\varepsilon<1$) if:

$$\frac{\sigma_{T_{IN}}}{\sqrt{N}} \le \varepsilon T_C \qquad (3)$$

i.e. by collecting at least

$$N^* = \left\lceil \frac{\sigma_{T_{IN}}^2}{\varepsilon^2 T_C^2} \right\rceil \qquad (4)$$

periods of the input 1-pps signal.

B. Analysis of the locking phase

As stated above, as soon as the circuit reaches the *locking phase*, the Counter 1 is switched to measure the time difference between the output and the input 1-pps signals. Such a difference can be either negative or positive depending on whether the output signal anticipates the input signal or not. If Δ_{T_i} is referred to as the delay between the output and input signals at the *i*th second of operation and Δ_{OUT_i} represents the jitter of the output period with respect to T_{ID} at the same time *i,* the difference between the output and input periods is

$$T_{OUT_i} - T_{IN_i} = \Delta_{OUT_i} - \Delta_{IN_i} = \Delta_{T_i} - \Delta_{T_{i-1}} \qquad (5)$$

Given that Δ_{T_i} is measured in terms of integer ticks k_i of the Counter 1, Δ_{T_i} can be expressed as

$$\Delta_{T_i} = k_i \cdot T_C \qquad (6)$$

On the other hand, the difference between the output periods at seconds *i* and *i*-1 is

$$T_{OUT_i} - T_{OUT_{i-1}} = \Delta_{OUT_i} - \Delta_{OUT_{i-1}} = (m_i - m_{i-1}) \cdot T_C \qquad (7)$$

where

$$m_i = m_0 - pk_{i-1} - l\sum_{j=1}^{i-1} k_j \qquad (8)$$

is the integer value produced by the PI controller to adjust the output signal period at time *i* and *p* and *l* are the proportional and integral parameters of the PI controller. In fact, using a PI controller is advantageous because the output period tends to track the possible long-term variations of the input, while the random jitter is filtered out. In order to prove this point, first of all observe that by combining (6) (7) and (8), (7) can be expressed as:

$$\Delta_{OUT_i} - \Delta_{OUT_{i-1}} = -(p + l) \cdot \Delta_{T_{i-1}} + p \cdot \Delta_{T_{i-2}} \qquad (9)$$

Then, from the z-transform of (5), it results that

$$\Delta_T(z) = \frac{\Delta_{OUT}(z) - \Delta_{IN}(z)}{1 - z^{-1}} \qquad (10)$$

Finally, by replacing (10) into the z-transform of (9), we obtain the following transfer function:

$$H(z) = \frac{\Delta_{OUT}(z)}{\Delta_{IN}(z)} = \frac{(p + l)z^{-1} - pz^{-2}}{1 + (p + l - 2)z^{-1} + (1 - p)z^{-2}} \qquad (11)$$

This transfer function describes an infinite impulse response (IIR) system exhibiting a low-pass behavior in the frequency domain. Notice that the filtering characteristics of the system depend on the chosen parameters *p* and *l* of the PI controller. In particular, such values can be optimized experimentally in order to minimize the output period fluctuations on the basis of the spectral features of the input jitter.

III. EXPERIMENTAL RESULTS

In order to validate the correct operation as well as the performance of the circuit described in Section II, the jitter of the 1-pps signal produced by a GPS receiver based on a module of moderate time stability has been measured and compared with the jitter of the same 1-pps stream regenerated by the synchronization circuit. To this purpose, the synchronization circuit has been implemented using an FPGA Xilinx Spartan XC3S200-4FT256. The proportional and integral parameters of the digital PI controller have been set as follows: $p=2^{-2}$ and $l=2^{-6}$, respectively. Such values are the closest powers of two enabling a unit-step response close to the critical damping of the system. This is essential to shorten the capture time of the circuit (i.e. below 30 s) and to reduce the rising time of the output pulse, thus improving the overall timing accuracy of the regenerated signal. The number of periods *N* collected in the transient phase has been set equal to 32, i.e. larger than $N^* \approx 30$ for ε=0.5 and $\sigma_{T_{IN}} \approx 30$ ns. Although using powers of two for *p* and *l* is not optimal for the PI controller design, this choice makes the hardware implementation simpler and faster, since just two shift registers instead of two hardware multipliers are required. As a consequence, the synthesized circuit is able to run at 100 MHz, while covering just 13% out of the available logic slices in the FPGA and 1% out of the total number of input-output blocks (IOBs). This is a significant result, because it implies that the circuit could be used as a component in a higher-level design, e.g. to synchronize to the GPS the operation of more involved digital signal processing components implemented inside the same FPGA. The correct operation and the performance of the synchronization circuit have been assessed through the measurement setup shown in Fig. 3. The GPS receivers used for the experiments are a high-accuracy, TCVCXO-disciplined Tekelec Epsilon board II, used as 1-pps time reference, and a less stable Ublox Antaris 4 LEA-4T GPS module, with a nominal worst-case jitter equal to 100 ns. In order to check the actual stability of the 1-pps signal used as a time reference, the time variations between two identical Tekelec Epsilon board II were preliminary compared in steady-state conditions [19]. In particular, after synchronizing the two Tekelec receivers to the GPS for 24 hours, their antennas were disconnected and the period differences between the two free-running 1-pps signals were measured for some hours. The histogram of such differences after compensating the systematic residual drift of the free-running TCVCXOs is shown in Fig. 4. Notice that the random jitter exhibits approximately a normal distribution. Also, the Allan standard deviation of the time variations over an observation interval of 2 s is about 0.5 ns, i.e. negligible compared to the target uncertainty. Given that the jitter values associated to the two Tekelec boards can be assumed to be independent and identically distributed (i.i.d.), the random period variations of the 1-pps signal can be equally assigned to each receiver. Hence, the random jitter of each Tekelec receiver can be assumed to be normally distributed with zero-mean and estimated Allan standard

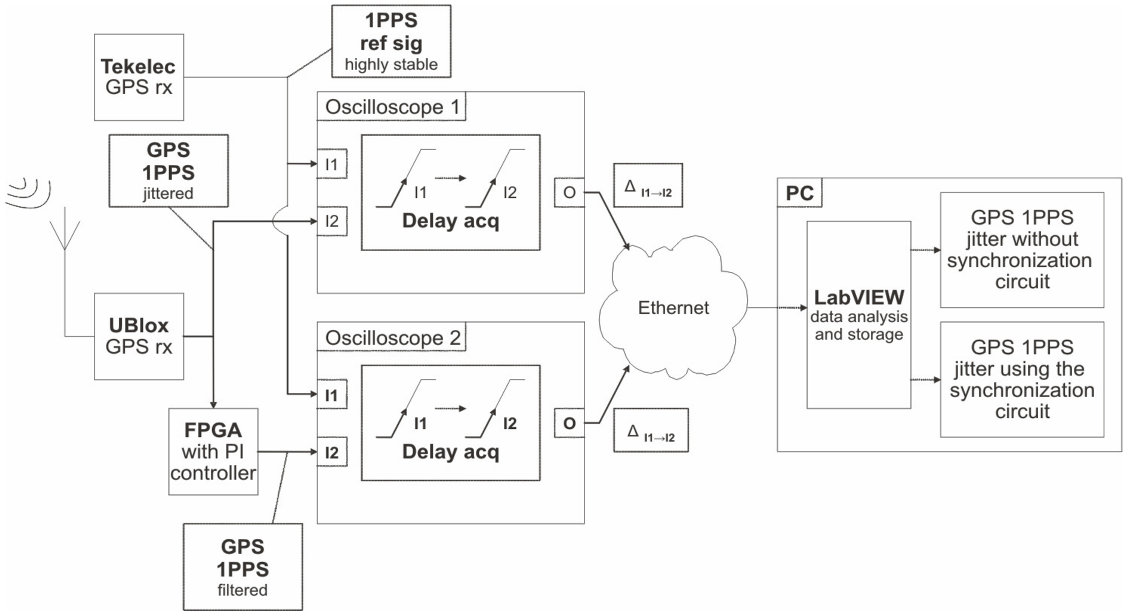

Fig. 3 - Block diagram of the measurement setup used for the experimental activity.

deviation equal 0.4 ns. Notice that this standard uncertainty is negligible compared to the nominal worst-case jitter of the 1-pps signals generated by the LEA-4T module. Therefore, the stability of the 1-pps stream produced by the Tekelec Epsilon board II is adequate as a time reference. Observe also that the Allan standard deviation has been used instead of the classical sampling standard deviation because the Allan estimator is more suitable to assess the frequency stability of a clock when the mean is changing [20].

After characterizing the 1-pps reference signal, the period variations between this signal and the 1-pps stream produced by the LEA-4T module before and after applying the synchronization circuit have been measured simultaneously using two digital storage oscilloscopes (DSO), i.e. a 500 MHz Tektronix TDS3052B and a 100 MHz Tektronix TDS3012B. In fact, both instruments are able to sample the input signals at a very high rate (i.e. larger than 1 GSa/s) and to perform time delay measurements through curve fitting and level crossing algorithms with a resolution smaller than 1 ns. Consider that the uncertainty contributions introduced by the experimental setup are not particularly significant, because the additional rise times due to the parasitic effects of the connections and to the dynamic performance characteristics of the DSO channels are much smaller than the intrinsic rise times of the pulses produced by the LEA-4T module. Also, the additional rise times due to the connections and to the analog sections of the two DSO channels tend to compensate each other when measuring the delay between the two waveforms. Such delay values have been collected and processed with a PC using NI LabView™ 7. In Fig. 5(a) and 5(b), the period variations measured over 1 hour before and after applying the synchronization circuit are shown. Observe that the variability of the time fluctuations in the output 1-pps signal is much smaller than in the input. In fact, the short-term Allan standard deviation over an observation interval of 2 s is reduced from 12.1 ns to 3.8 ns (i.e. by more than 60%). This confirms the effectiveness of the proposed approach.

IV. CONCLUSION

This paper deals with a simple synchronization circuit that is able to reduce the jitter of the 1-pps signal generated by a low-cost GPS receiver with low accuracy. The main advantage of the proposed solution is that it can be easily implemented in a fully digital device such as an FPGA. Moreover, the time to lock the input signal is much shorter than in more expensive TCVCXO-based solutions. The jitter reduction is mostly due to the filtering capabilities of the PI controller used within the circuit. The use of a low-cost FPGA and the reduced size of the proposed circuit also enable the implementation of other network interfaces and control functions within the same component.

V. ACKNOWLEDGMENTS

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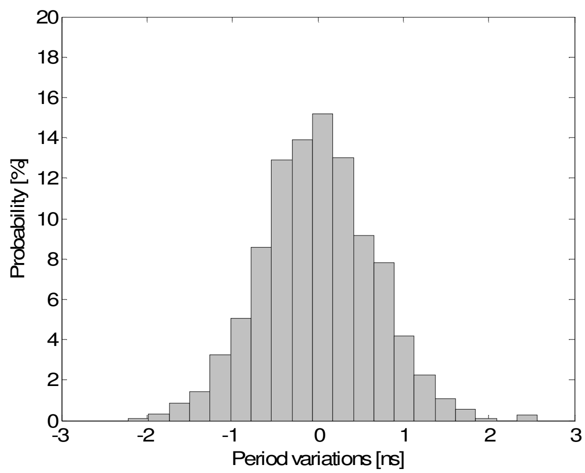

Fig. 4 – Histogram of the random jitter affecting two high-accuracy TCVCXO-disciplined GPS receivers Tekelec Epsilon Board II, after compensating the systematic trend.

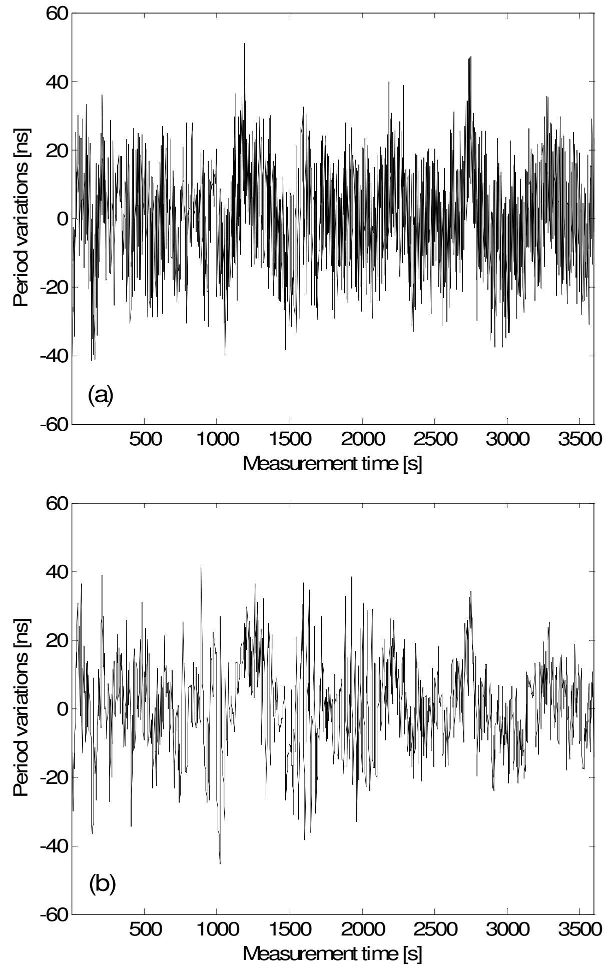

Fig. 5 – Time differences between the rising edges of a high-accuracy 1-pps signal generated by a Tekelec Epsilon board II used as a time reference and the rising edges of a less accurate Ublox Antaris 4 LEA-4T GPS module before (a) and after (b) applying the synchronization circuit.

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